

REMARKS

In the Office Action, the Examiner rejected Claims 1, 12, 13 and 14 under 35 U.S.C. 102 as being fully anticipated by a document "Single Electron Switching Events in Nanometer-Scale Si MOSFET's" (Howard, et al.). Claims 2-11 and 31-45 were allowed. The Examiner objected to Claims 15-30 as being dependent upon a rejected base claim, and indicated that these claims also would be allowable if appropriately re-written.

The Examiner, in the Office Action, also objected to the specification and to the language of Claim 1. In particular, the Examiner asked that the specification be amended to update the status of the parent application, and that Claim 1 be amended to insert "and" before the last step of the claim.

Independent Claims 1 and 12 are being amended to better define the subject matters of these claims. Claim 15 is being rewritten in independent form including the limitations of previous Claims 12 and 13.

The specification is being amended to update the reference, on page 1, line 5, to the parent application, and specifically, to indicate that the parent application is now abandoned. In view of this change, the Examiner is asked to reconsider and to withdraw the objection to the specification.

Also, Applicants wish to note that, in amended Claim 1, "and" is included before the last step of the claim. It is believed that this overcomes the Examiner's objection to the language of Claim 1, and the Examiner is requested to reconsider and to withdraw the objection to the language of Claim 1.

In addition, for the reasons discussed below, Claims 1 and 12-30 patentably distinguish over the prior art and are allowable. The Examiner is, accordingly, respectfully requested to reconsider and to withdraw the rejections of Claims 1, 12, 13 and 14 and the objections to Claims 15-30, and to allow Claims 1 and 12-30.

The present invention, generally, relates to the analysis of operating integrated circuits. In this analysis, information, such as switching and timing data, is obtained about the activities of individual circuit elements, and that information can then be used to learn about the integrated circuits. In particular, this involves using a technology that performs logic and timing analysis within circuit components.

Howard, the only reference relied on by the Examiner to reject Claims 1 and 12-14, describes a low-speed measurement, using a standard current vs. voltage measurement to discover the quantity of interface traps in drains of transistors. These transistors are fabricated on test parts to determine the defect density that may occur on a production IC. The method they describe is to design specific device structures (not applicable to production ICs), and perform a slow measurement that counts changes in the drain conductance of these devices with the voltage probe in order to determine the number of electrons held in traps in the drain. Their method is to modulate voltage and temperature in order to calculate the number of electrons trapped.

The present invention, in its preferred implementation, is designed to measure product ICs. These are operated at the specified conditions for the part. In addition, the present invention does not require a standard voltage measurement against voltage and temperature. Instead, this invention measures emissions from actively switching transistors in order to determine the speed of both gate-to-gate performance, and also the slew rate of individual transistors. The invention is directed to characterizing circuit activity, rather than monitoring defects, as in Howard.

In paragraph 8 of the Office Action, the Examiner cites section IV of Howard. This section describes a lock-in amplifier method for measuring frequency response is described.

The present invention does not measure frequency response. Instead, the invention measures the time and location of switching events and maps these to the design layout and expected signal

propagation through the circuit.

Section VI of Howard is also cited in the Office Action. In this section, the authors conclude that by using temperature and gate voltage modulation, they may provide a direct measure of the activation energy in traps. They also teach that their method may be used to understand the quantity of noise (or variability) in transistor devices as they scale.

The instant invention does not measure modulation or device scaling properties. It is respectfully submitted that Howard does not teach a method to measure spatial and temporal measurement of an active IC, as the present invention does.

With particular regard to Claims 15, this claim, as mentioned above, is being rewritten in independent form including the limitations of previous Claims 12 and 13. Claim 15 positively sets forth the feature that the switching data is comprised of photon emissions and the IC design viewer is enabled to display emission images. As it is believed that Examiner has recognized, this feature represents an important, patentable advancement, and is not disclosed in or suggested by Howard, et al, or any of the other references of record. Accordingly, Claim 15 and Claims 16-30, which are dependent from Claim 15, patentably distinguish over the prior art and are allowable. The Examiner is, consequently, respectfully requested to reconsider and to withdraw the objection to Claims 15-30, and to allow these claims.

Also, independent Claims 1 and 12 are being amended to describe important features of the invention that are not shown in or suggested by the prior art. Specifically, Claim 1, which is directed to a method for characterizing switching behavior in an integrated circuit, describes the steps of generating and applying signals to an integrated circuit to cause repeated switching activity in a region of interest in the integrated circuit, wherein said switching activity generates emissions from that region of interest, and resolving this switching activity in both space and time.

Claim 12 is directed to a system for characterizing switching behavior in integrated circuits. Claim 12, as presented herewith, describes means for generating and applying signals to an integrated circuit to cause repeated switching activity in a region of interest in the integrated circuit, wherein said switching activity generates emissions from that region of interest, and means for resolving this switching activity in both space and time.

These features are not shown in or suggested by Howard, et al, which is directed to monitoring defects, rather than characterizing circuit activity.

The other references of record have been reviewed, and these other references, whether considered individually or in combination, also do not disclose or suggest the above-described features of the present invention.

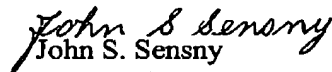
For example, U.S. Patent 5,825,191 (Nijima, et al.) discloses an IC fault location tracing apparatus. This apparatus uses a combination of a semiconductor IC tester, a charged particle beam tester, and CAD data produced in the design stage of the IC device. A control device is provided that stores net list data and mask layout data.

The instant invention operates in a completely different way. In contrast to the broad electron beam analysis employed in Nijima, the present invention characterizes and analyzes information about individual switching events.

Because of the above-discussed differences between Claims 1 and 12 and the prior art, and because of the advantages associated with these differences, these claims patentably distinguish over the prior art and are allowable. Claims 13 and 14 are dependent from Claim 12 and are allowable therewith. Accordingly, the Examiner is requested to reconsider and to withdraw the rejections of Claims 1, 12-14, and to allow these claims.

For the reasons set forth above, the Examiner is requested to reconsider and to withdraw the objections to the specification and to the language of Claim 1. The Examiner is further asked to reconsider and to withdraw the rejections of Claims 1, 12, 13 and 14 under 35 U.S.C. 102, and the objections to Claims 15-30, and to allow Claims 1 and 12-30. If the Examiner believes that a telephone conference with Applicants Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully Submitted


John S. Sensny
Registration No. 28,757
Attorney for Applicants

Scully, Scott, Murphy & Presser, P.C.
400 Garden City Plaza – Suite 300
Garden City, New York 11530
(516) 742-4343

JSS:jy